IN THE CLAIMS:

1. (original) A method for performing Incremental Redundancy (IR) operations in a wireless receiver comprising:

receiving an analog signal corresponding to a data block;

sampling the analog signal to produce samples;

equalizing the samples to produce soft decision bits of the data block;

configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers;

initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver; and

accessing, by the IR processing module, the plurality of IR processing module registers; and

performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block.

2. (original) The method of claim 1, wherein the data block comprises a complete link layer data block.

3. (original) The method of claim 1, wherein configuring the plurality of IR processing module registers comprises the system processor writing the soft decision bits of the data block to the plurality of IR processing module registers.

4. (original) The method of claim 1, further comprising the system processor writing the soft decision bits of the data block to a memory accessible by the IR processing module.

5. (original) The method of claim 1, wherein performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block further comprises the IR processing module:

determining that an additional copy of the data block is stored in memory;

retrieving soft decision bits of the additional copy of the data block;

soft combining the soft decision bits of the additional copy of the data block with the soft decision bits of the data block to produce combined soft decision bits of the data block; and

decoding the combined soft decision bits of the data block.

6. (original) The method of claim 5, wherein:

determining that an additional copy of the data block is stored in memory is based upon type I IR memory contents; and

retrieving soft decision bits of the additional copy of the data block includes accessing type II IR memory.

7. (original) The method of claim 5, further comprises the IR processing module identifying an IR mode of the additional copy of the data block stored in memory.

8. (currently amended) The method of claim 7, further comprising, the IR processing module:

identifying a puncturing pattern of the additional copy of the data block stored in memory; and

depuncturing the copy of the data block stored in memory, ~~if~~ when required.

9. (original) The method of claim 5, further comprising assigning different weights to each of the data block and the additional copy of the data block for soft combining.

10. (original) The method of claim 9, wherein weights are assigned to the data block and to the additional copy of the data block based upon respective measured signal qualities.

11. (original) The method of claim 5, further comprising the IR processing module storing the combined soft decision bits of the data block in memory for later use.

12. (original) The method of claim 1, wherein the IR operations performed by the IR processing module include:

decoding the soft decision bits of the data block to produce a decoded header; and

identifying a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block from the decoded header;

depuncturing the soft decision bits of the data block based upon the MCS mode and puncturing pattern to produce depunctured soft decision bits; and

decoding the depunctured soft decision bits.

13. (original) The method of claim 1, further comprising storing the soft decision bits of the data block in IR memory.

14. (original) The method of claim 1, further comprising the IR processing module:

failing to correctly decode a header of the data block; and

discarding the soft decision bits of the data block.

15. (original) The method of claim 1, wherein:

each symbol of the data block is represented by four punctured soft decision bits; and

each symbol of the data block is also represented by five depunctured soft decision bits.

16. (original) A system for implementing Incremental Redundancy (IR) operations in a wireless receiver comprising:

a baseband processor that is operable to receive analog signals corresponding to a data block and to produce samples of the analog signals;

an equalizer that is operable to receive the samples from the baseband processor, to equalize the samples, and to produce soft decision bits of the data block;

a system processor that is operable to receive the soft decision bits of the data block;

a plurality of IR processing module registers communicatively coupled to the system processor;

an IR processing module communicatively coupled to the system processor and to the plurality of IR processing module registers;

wherein the system processor is operable to configure the plurality of IR processing module registers and to initiate operation of the IR processing module of the wireless receiver; and

wherein the IR processing module is operable to access the plurality of IR processing module registers, to receive the soft decision bits of the data block, and to perform IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block.

17. (original) The system of claim 16, wherein the data block comprises a complete link layer data block.

18. (original) The system of claim 16, wherein in configuring the plurality of IR processing module registers, the system processor writes the soft decision bits of the data block to the plurality of IR processing module registers.

19. (original) The system of claim 16, wherein the system processor is further operable to write the soft decisions of the data block to a memory accessible by the IR processing module.

20. (original) The system of claim 16, wherein in performing IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block, the IR processing module is operable to:

determine that an additional copy of the data block is stored in memory;

retrieve soft decision bits of the additional copy of the data block;

soft combine the soft decision bits of the additional copy of the data block with the soft decision bits of the data block to produce combined soft decision bits of the data block; and

decode the combined soft decision bits of the data block.

21. (original) The system of claim 20, wherein the IR processing module is further operable to:

determine that an additional copy of the data block is stored in memory based upon type I IR memory contents; and

retrieve soft decision bits of the additional copy of the data block by accessing type II IR memory.

22. (original) The system of claim 20, wherein the IR processing module is further operable to identify an IR mode of the additional copy of the data block stored in memory.

23. (currently amended) The system of claim 22, wherein the IR processing module is further operable to:

identify a puncturing pattern of the additional copy of the data block stored in memory; and

depuncture the copy of the data block stored in memory, ~~if~~ when required.

24. (original) The system of claim 20, wherein different weights are assigned to each of the data block and the additional copy of the data block for soft combining.

25. (original) The system of claim 24, wherein weights are assigned to the data block and to the additional copy of the data block based upon respective measured signal qualities.

26. (original) The system of claim 20, wherein the IR processing module is further operable to store the combined soft decision bits of the data block in memory for later use.

27. (original) The system of claim 16, wherein the IR processing module is further operable to:

decode the soft decision bits of the data block to produce a decoded header; and

identify a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block from the decoded header;

depuncture the soft decision bits of the data block based upon the MCS mode and puncturing pattern to produce depunctured soft decision bits; and

decode the depunctured soft decision bits.

28. (original) The system of claim 16, wherein the IR processing module is further operable to store the soft decision bits of the data block in an IR memory.

29. (original) The system of claim 16, wherein the system processor is further operable to store the soft decision bits of the data block in an IR memory.

30. (original) The system of claim 16, wherein the IR processing module is further operable to:

fail to correctly decode a header of the data block; and

discard the soft decision bits of the data block.

31. (original) The system of claim 16, wherein:

each symbol of the data block is represented by four punctured soft decision bits; and

each symbol of the data block is also represented by five depunctured soft decision bits.